Critical Success Factors: Fabless-Foundry Collaboration
- Xilinx 28nm product development case study

Xin Wu, Senior Director, Silicon Technology
Xilinx, Inc.
Agenda

- 28nm Case Study Overview

- HPL Process & 2.5D SSI Technology Development
  - Key Milestones
  - Power-Performance-Area
  - Test Chips
  - Initial Ramping & Feedback

- Summary
28nm Design Objective:
Breakthrough in Optimization & Integration

Market Optimization

- Extreme Bandwidth & Capacity
- Performance
- Price/Perf/Watt
- Price & Power

Logic Integration
Serdes Integration
Processing Integration

VIRTEX
System Optimized w/ SSIT

KINTEX

ARTIX

ZYNQ

Programmable System Integration

© Copyright 2012 Xilinx
Close Collaboration with Technology Partners
28nm HPL Process Optimized for FPGAs

TSMC / Xilinx Collaboration for Superior Performance per Watt

Higher Performance, Lower Leakage

28HPL
Optimal for FPGAs

28LP
Best for Cell Phones

28HP
Best for GPUs
Close Collaboration with Technology Partners

**Xilinx 7-Series SSIT Supply Chain**

- Partner with both TSMC and Amkor to develop SSIT
- Ramping sample volume in both TSMC and Amkor
- Shipping 100’s of Engineering Samples to Top Key Customers

- FPGA, Interposer, & Package Design
- 28nm FPGA & Interposer
- Package Substrate
- Dual Sources
- μBump, CoW attach
  - Die separation, & Assembly
- μBump, Die separation
  - CoC attach, & Assembly
- Final Test, Verification and Qualification
Key 28nm Milestones

Technical collaboration throughout the product lifecycle

As of Nov 2011

Models

28HPL definition

Drules/PDKs

TVs & Si

As of Nov 2011

Readiness Reviews

Products
Achieving Power-Performance-Area Goals

- Critical areas of technology definition, constantly monitored/driven

<table>
<thead>
<tr>
<th>Process Choice</th>
<th>28HP</th>
<th>28HPL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Power</td>
<td>2.21x</td>
<td>1.0x</td>
</tr>
<tr>
<td>Fabric Performance</td>
<td>1.02x</td>
<td>1.0x</td>
</tr>
</tbody>
</table>

Actual Hardware Results

<table>
<thead>
<tr>
<th>Static Power</th>
<th>Total Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.6W</td>
<td>6.5W</td>
</tr>
<tr>
<td>0.8W</td>
<td>3.1W</td>
</tr>
</tbody>
</table>

Kintex™-7 FPGA Power Estimator
28nm Si Technology Development Test Chips

Enabling early detection of design-related issues

TV0: technology path finder
TV1: Integration and basic devices
TV2: Basic elements: RAM, RF, StdCel, etc
TV3/PPLV: Circuit blocks, process-design interactions, pilot prep
TV4 & 5: More circuit blocks, & later products

2008  2009  2010  2011

28nm starts

© Copyright 2012 Xilinx
## 7-Series 3D-IC Test Chips

*Enabling early detection of design-related issues*

<table>
<thead>
<tr>
<th>Test Vehicle</th>
<th>CY09</th>
<th>CY10</th>
<th>CY11</th>
<th>CY12</th>
</tr>
</thead>
<tbody>
<tr>
<td>TV1 (90nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TV2 (40nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TV3 (28nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7V2000T (28nm)</td>
<td>ISE Beta</td>
<td>TO</td>
<td>ES</td>
<td>Prod</td>
</tr>
</tbody>
</table>

- Module Development ✓
- Process Integration ✓
- Reliability Assessment ✓
- Supply Chain Validation ✓
- Design Enablement ✓
- Design Validation ✓
- Process Qualification ✓
- EA Design Tools ✓
- Initial Sampling ✓
7-Series 3D-IC Test Chips (cont’d)

Enabling early detection of design-related issues.

Aswan2A/2B are 28Gbps SERDE testchip, normal flipchip package vs. via a SSIT connection. The Si data shows comparable results.
Initial Ramping

- FPGA enables accelerated learning: hours vs. months

FAB | FPGA
---|---
Advanced In-Line Inspection | Wafer Sort
Yield Improvement | Root Cause Analysis

> 3 months
Initial Ramping (2)

FPGA architecture drives yield & quality improvements

FPGA is a Powerful Yield Learning Vehicle with Multiple layers of Programmable Features that can effectively:

- **Defect Reduction**
  - Quick to detect defects
  - *If you can’t find it, you can’t fix it*

- **Process Control**
  - Powerful to measure variations
  - *If you can’t measure it, you can’t improve it*
Summary

➤ Staying at the leading edge is not for everyone
  – There’s no “one-size-fits-all” approach to advanced technology development & ramping to volume

➤ Xilinx brings 25+ years experience with foundries & OSATs:
  – Tightly collaborate with the supply chain
  – Apply proven tools & methodologies to achieve product goals
  – Exploit advantages and avoid weaknesses to achieve win-win results

➤ Technology advancements benefit the industry at large
  – Communications & best practice sharing at events such as ConFab are key!

THANK YOU

Follow Xilinx on:

facebook.com/XilinxInc
twitter.com/#!/XilinxInc
youtube.com/XilinxInc

© Copyright 2012 Xilinx