The Technology And Cost To Implement Next Generation Device Technologies.

Mark Thirsk
Linx Consulting
Overview

- Major technological challenges
- Maturing industry with slower growth
- Cost challenges
- EUV and 450mm
- Rapid introduction of new materials

Linx Consulting and IC Knowledge have developed a unique modeling capability that can evaluate these scenarios in a detailed and self-consistent manner.
The Markets We Serve

Electronics Imports

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Econometric Forecast

Shaded areas indicate US recessions

Annual Percent Change
2010 2011 2012 2013f 2014f 2015f
39.7 -3.5 -0.1 3.3 9.8 8.1

<table>
<thead>
<tr>
<th>Q2 2013 Forecast (May 2013)</th>
<th>2013Q1</th>
<th>2013Q2F</th>
<th>2013Q3F</th>
<th>2013Q4F</th>
<th>2014Q1F</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSI</td>
<td>2128</td>
<td>2380</td>
<td>2495</td>
<td>2329</td>
<td>2334</td>
</tr>
<tr>
<td>%Change</td>
<td>-1.6%</td>
<td>11.8%</td>
<td>4.8%</td>
<td>-6.7%</td>
<td>0.2%</td>
</tr>
</tbody>
</table>
Notes:
1. X axis is on a percentage basis
2. Size of box is proportional to wafer starts
3. Source: Semico and Linx estimates
≥90nm devices are growing at a rate much closer to GDP, driven by a different set of end markets.
The Major Challenges For ICs

- New Memory
- 3D Packaging
- Gate Architecture
- HIGH MOBILITY CHANNEL
- Ge
- IIIIV
- 32nm High-K CMOS
- 11 level metal
- Deep trench capacitor
- Cu Through Silicon Via (TSV)
- EUV
Device Challenges

- **Logic**
  - Planar scaling is at an end
  - Move to fully depleted devices with FDSOI or MG
  - Migrate to new materials, Ge - PMOS, III/V – NMOS channels
  - New devices - tunnel FETs, nanowires, gate all around - in the long term

- **Volatile memory**
  - DRAM capacitor scaling challenges
  - MRAM is coming is sooner than previously expected

- **Non-volatile memory**
  - NAND 2D to 3D transition
  - Long term RRAM
  - PCRAM can’t meet the density of NAND but will find applications replacing NOR and as storage class memory
2018 - 450mm production ramp
Process complexity is driving higher growth in materials demand than the wafer start growth.
- The BOM component of semiconductor sales will increase over the next 5 years, and fall as 450mm grows.

- Photoresist and Ancillaries become a major component of the overall BOM.

- Vapor deposition will continue to displace physical deposition, driving growth of ALD and CVD materials.
Current process technology diverges from the historic cost per bit curve as multi patterning and process complexity increase.

EUV reduces this divergence by reducing litho complexity and saving some patterning cost.

Combining EUV with 450mm allows the cost per bit to stay on trend.
Long Term EUV Forecast

Exp. / year 000s

Tool Count – dashed lines

300mm Exp Demand
450mm Exp Demand
300mm Tool Count
450mm Tool Count
### EUV Wafer Cost Impact

<table>
<thead>
<tr>
<th>Year</th>
<th>With EUV</th>
<th>No EUV</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ASIC</td>
<td>DRAM</td>
</tr>
<tr>
<td></td>
<td>M1 ½ Pitch</td>
<td>Cost per Wafer</td>
</tr>
<tr>
<td>2014</td>
<td>With EUV</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td>No EUV</td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td>With EUV</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>No EUV</td>
<td></td>
</tr>
<tr>
<td>2016</td>
<td>With EUV</td>
<td>18.9</td>
</tr>
<tr>
<td></td>
<td>No EUV</td>
<td></td>
</tr>
</tbody>
</table>

Modeling 300mm in South Korea
30,000 wpm Fab
450mm Wafer Cost Impact

**DRAM Wafer Cost Trend**

- 300mm
- 450mm
- 23%
- 450mm starting wafer

**NAND 2D Wafer Cost Trend**

- 300mm
- 22%
- 450mm
- 450mm starting wafer

**MPU Wafer Cost Trend**

- 300mm
- 26%
- 450mm

**Korea**
- 60k wpm (300mm)
- 90k wpm (450mm)

**Korea**
- 100k wpm (300mm)
- 150k wpm (450mm)

**US**
- 30k wpm (300mm)
- 45k wpm (450mm)
## New Materials Needs

<table>
<thead>
<tr>
<th>Applications</th>
<th>Materials</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Vapor Deposition</strong></td>
<td></td>
</tr>
<tr>
<td>Stressors</td>
<td>Chlorosilanes for stress films for logic devices.</td>
</tr>
<tr>
<td>Silanes</td>
<td>Disilane as a precursor to grow high quality polysilicon/silicon films.</td>
</tr>
<tr>
<td>Ge and Germane</td>
<td>Channel stress and electrode. High mobility gate material.</td>
</tr>
<tr>
<td>Dielectric CVD</td>
<td>Low-k dielectric methyl silanes High k layer precursors for Hf, Zr, lanthanides, and chalcogenides.</td>
</tr>
<tr>
<td>Metal CVD / ALD</td>
<td>Ta, Ti, Co, Cu precursors for HKMG, interconnect, MIM, and 3D.</td>
</tr>
<tr>
<td>Compound Semis</td>
<td>Al, Ga, and In MOCVD and epitaxial precursors, as well as Grp V complements.</td>
</tr>
<tr>
<td>TSA</td>
<td>Advanced gapfill processes (STI and PMD) in logic and memory.</td>
</tr>
<tr>
<td><strong>Litho</strong></td>
<td></td>
</tr>
<tr>
<td>DSA Materials</td>
<td>Block copolymers for lithography extension</td>
</tr>
<tr>
<td>Spin on Hard Masks</td>
<td>High Carbon etch mask, or spin on silicon based hardmasks.</td>
</tr>
<tr>
<td>EUV Resists</td>
<td>Low LWR resists</td>
</tr>
<tr>
<td><strong>Cleaning</strong></td>
<td></td>
</tr>
<tr>
<td>PERR</td>
<td>Interconnect cleaning</td>
</tr>
<tr>
<td>PCMP</td>
<td>Novel formulations with reduced amine CsOH use</td>
</tr>
<tr>
<td>III/V HEMT</td>
<td>Solvent and aqueous cleans, including contact cleans Sulphur and Hydrogen surface termination, or H&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;2&lt;/sub&gt; vapor clean</td>
</tr>
<tr>
<td>TSV</td>
<td>Post etch cleans, bonding adhesive removal, bump resist removal.</td>
</tr>
<tr>
<td>Mask Cleans</td>
<td>Defect reduction and cleaning on EUV masks</td>
</tr>
<tr>
<td>CMP</td>
<td>Novel slurries for HEMT</td>
</tr>
</tbody>
</table>
EUV Litho Challenges

- Source Power Challenge
  - Multiple road map delays
  - Difficult engineering challenges
  - All the eggs in one basket now

- Resist Challenges
  - Atomic absorption
  - Thin resist films
  - Ancillary Layers
  - Stochastic noise and LWR targets

- Mask Clean Technologies
  - Creation of perfect mask blanks
  - No added defects on processing
  - Cleaning and metrology challenges
Supply Chain Optimization

- Increasing Focus on formulation sub-suppliers
- Evaluating strategic supplier readiness
- Imposed significant fines for quality manual violations
- Actively eliminating under performing suppliers

<table>
<thead>
<tr>
<th>IMPACT to:</th>
<th>Raws</th>
<th>Qualified Product</th>
<th>On Wafer</th>
<th>Packed Chips</th>
<th>Consumer Product</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Business</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Good Will</td>
<td>![Image]</td>
<td>![Image]</td>
<td>![Image]</td>
<td>![Image]</td>
<td>![Image]</td>
</tr>
<tr>
<td><strong>Technical</strong></td>
<td></td>
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<tr>
<td>ID Root Cause</td>
<td>![Image]</td>
<td>![Image]</td>
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<td>![Image]</td>
<td>![Image]</td>
</tr>
</tbody>
</table>
Conclusions

- Growth returns in 2013, but is moderate for the medium term.
  - Overall market growth is reducing.

- A high growth potential remains in advanced segments which will require specialty materials.
  - This is offset by significant R&D requirements.
  - HKMG, FinFETs, FDSOI, 3D-NAND and STT-MRAM development programs are already well advanced, although challenges remain at 22nm and below.

- More Moore has significant implications for both equipment and materials suppliers.
  - 450mm is driven by fab economics. Prepare for deployment over the next 5 years.
  - 450mm will probably slow materials market volume growth, but require advanced materials.
Conclusions

- EUV is needed to mitigate lithography complexity and keep wafer cost low. Challenges of source power gate implementation.
- Materials demand grows faster than Semiconductor Unit growth due to process complexity.
  - Patterning, CVD and ALD, and CMP all drive materials demand growth.
- 3D Packaging and TSV processing is a key area for focus over the next 5 years.
- Supply Chain Management is becoming a critical competence for materials suppliers.
IC-Knowledge

Strategic Cost Model - equipment edition - easily project wafer cost and equipment requirements for the next 15 years based on the ITRS. Allows extensive process and equipment customization.

IC-Knowledge & Linx Consulting

Strategic Cost Model - materials edition - easily project wafer cost, equipment and materials requirements for the next 15 years based on the ITRS. Allows extensive process, material and equipment customization.

Linx Consulting

Econometric Semiconductor Forecast – monthly forecasts of silicon area demand developed in collaboration with Hilltop Economics LLC.
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