Applications Drive Packaging Challenges in Growth Markets
Growth Areas for Application Specific Packaging

- Highest growth in applications that have unique constraints for packaging
  - Constraints very different than traditional CPU and other classic packaging
    - Thickness
    - X, Y size
    - Thin die
    - Sensors, MEMS, Cameras
    - Integrated Antennas and Shielding
- Packaging solutions driven by these constraints
  - Stacked packages
  - WLP
  - Modules
    - Embedded active and passives
  - FOWLP
  - 2.5 and 3D
  - ????
- Tight collaboration required in supply chain
Mobile package styles (Nexus 4 Phone Board)

- Power Management IC PM8921 WLP Package
- LTE Modem MDM9515M Flip Chip Hybrid Package
- Application Processor APQ8064 MLP PoP Package
- Memory
- Apps Proc
- PWB

Fine Pitch Packages (≤0.4mm BGA pitch, up to 1000 I/O, in <15mm package)
Advanced Mobile Package Structures

POP (package on package)
Molded Laser PoP (MLP)

FC CSP
Flip Chip/Wire bond or Hybrid

WLP

Modules (actives and passives)
Embedded die module

FOWLP (fan out WLP)
Handset Thickness Decreasing Over Time - where will it stop?

Other Trends
- Area Increasing, Larger Screens
- Battery Volume Constant
- Phone Volume decreasing, but stabilizing

<table>
<thead>
<tr>
<th>Year</th>
<th>mm</th>
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<tbody>
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<td>2006</td>
<td>13</td>
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<td>2007</td>
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<td>7</td>
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<td>2013</td>
<td>6</td>
</tr>
<tr>
<td>2014</td>
<td>?</td>
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</table>
Thickness Comparison of Qualcomm Mobile Packages

Includes BGA Balls

Standard issue US Penny

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*PoP Package thickness includes memory
Technical Challenges for Mobile Applications

**Materials and Processes**
- New substrate technologies (ETS)
- Fine pitch Cu Pillars/uBumps (<100um pitch)
- Low CTE, High Modulus Substrate Materials
- High CTE Mold Materials

**Thermal Challenges**
- Higher Tj (>100°C)
- Poor thermal paths
- No air flow. Closed system
- 3D integration

**Mechanical Challenges**
- Thin die (<150um)
- CTE mismatch and CPI
- Warpage Control
- Preserving Si Strain Eng. And E. Perf. (eCPI)

**Electrical Challenges**
- Signal Integrity
- Power Distribution Network
- Functional Partitioning

Application Drives Balance Point
FC CSP Package Structure

- Package constituents of similar thicknesses but different CTEs
  - Warpage difficult to control
- Solder balls are a significant fraction of the total package height

Not to Scale
Typical Dimensions

0.5mm pitch

0.4mm pitch

150um pitch

Bare die FC PoP package with stacked memory
Interconnect Trends for Mobile Packages

- Substrate uses narrow bond leads instead of flip chip pads, and die uses Cu pillars with SnAg solder cap
  - CuBOL: Cu pillar bond on lead mass reflow chip attach
  - TCFC: thermo-compression flip chip attach
  - CuBOL/ETS – coreless embedded trace substrate with BOL interconnect
  - Capillary and molded underfills are used

Conventional solder bump flip chip

Mass Reflow FC (≥140 um)
CuBOL/ETS (≥100 um)
CuBOL (>100 um)
TCFC (≤80 um)
## Substrate manufacturing trends – Strip based

<table>
<thead>
<tr>
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<th>2008 HVM</th>
<th>Current 2014 HVM</th>
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<tr>
<td>Patterning Method (um)</td>
<td>mSAP (30/30)</td>
<td>SAP (15/15)</td>
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<tr>
<td>Min FC Pitch (um)</td>
<td>150</td>
<td>40/80</td>
</tr>
<tr>
<td>Core material CTE (ppm)</td>
<td>15</td>
<td>3</td>
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<tr>
<td>Via count per panel</td>
<td>1x</td>
<td>2x</td>
</tr>
<tr>
<td>Layer count</td>
<td>2L &amp; 4L</td>
<td>1.5L, 2L, 4L &amp; 6L</td>
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<tr>
<td># of Mfg Steps</td>
<td>1x (2L)</td>
<td>3x (6L)</td>
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<tr>
<td>Decoupling solution</td>
<td>None</td>
<td>Embedded Capacitors</td>
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<tr>
<td>Buildup dielectric</td>
<td>Prepreg</td>
<td>Prepreg, ABF</td>
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<tr>
<td>Coreless</td>
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<td>Prepreg, ETS</td>
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Future Technologies: FOWLP, Modules, 2.1, 2.5, 3D, ?
The Quest for smaller form factor and higher integration

• FO-WLP
  – Eliminates die interconnect (bump and wirebonds) and substrate
    – Shorter interconnects = Lower parasitics
    – Eliminate interconnect stress and ELK crack delamination issues
  – Batch packaging process like WLP, but can be with KGD
  – Potential SiP, Multi-die, 3D Solution

• Modules
  – Higher component density – saves PWB area
  – Can deal with finer pitches than standard SMT line
  – Embedded devices enables 3D

• 2.1 and higher D’s
  – Shorter interconnects = Lower parasitics
  – Interconnect pitches approaching wafer BEOL
  – Structures enabled by all of the above technologies
TSMC’s InFO WLP

- Integrated with advanced silicon process and chip-PKG co-design
- Ultra-fine pitch RDL (highest in industry) with ultra-thin (0.25mm) package body
- 225mm² pkg. size qualified for single chip and 64mm² pkg. size qualified for multi-chip scheme
- Ultra-high Q (~60) built-in inductor
- Enable ultra-thin PoP for high-performance mobile applications
- Short design/production cycle time and time to market

Courtesy of TSMC
Embedded Substrate Description

Key Features

- Component placed at the center of the thickness direction of substrate
  - Warpage resistive
  - Good compatibility with conventional PCB process (lamination and laser via process)

- No special equipment or foreign adhesive material inside the structure
  - Conventional SMT machine or FC bonder modified for large working and thin panel
  - No adhesive resin used but only PCB resin is filled in the space (simple and highly reliable)

- Enhanced power stability using both side interconnection of blind via (figure c)

Courtesy of SEMCO (ACI group)
TDK SESUB Battery Charging Module

- Charge/input current: up to 4A
- Input voltage range: 3.7V to 15V
- Automatic DC Input evaluation
  - Automatic Power Source Detection
  - Automatic Input Voltage Detection
  - Automatic Input Current Limit
- Can support QuickCharge2.0 for 75% faster charging time
- Automatic float voltage compensation

<table>
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<tr>
<th>Term</th>
<th>Description</th>
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<tbody>
<tr>
<td>APSD</td>
<td>Automatic Power Source Detection (USB BC1.2)</td>
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<tr>
<td>AICL</td>
<td>Automatic Input Current Limit</td>
</tr>
<tr>
<td>AFVC</td>
<td>Automatic Float Voltage Control</td>
</tr>
<tr>
<td>AIVD</td>
<td>Automatic Input Voltage Detection</td>
</tr>
<tr>
<td>HVDCP</td>
<td>High Voltage Dedicated Charging Port</td>
</tr>
</tbody>
</table>

User pad: 0.5mm pitch
13x10 matrix
94 pads

Courtesy of TDK
2.5D / 3D Stacking Roadmap

**Current Focus:** Wide IO DRAM on Logic = TSS

**Next:** Logic on Logic / Interposer / Both …

In Production: POP

3D Integration Levels

- POP LPDDRx on Logic
- W/B & FC Bump Stacking
- Interposer Logic & DRAM
- Interposer Heterogeneous
- TSS WideIO DRAM with Logic
- TSS WideIO Memory on Logic
- TSS Logic on Logic
- TSS Everything

Phone driven

Not-Phone driven

Vertical Stacking

Side by Side Stacking

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Courtesy of Matt Nowak, Riko Radojcic and Urmi Rey - Qualcomm
Thank You