Why 2.5D and 3D Semiconductors are Changing Everything

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The Effect of 2.5/3D on Devices

Graph showing the growth of transistors and frequency with and without 3D technology from 1960 to 2020.
Span of 3D Integration

Packaging

3D Through Via Chip Stack

Tezzaron
3D-ICs
100-1,000,000/sqmm
1000-10M Interconnects/device

Peripheral I/O
- Flash, DRAM
- CMOS Sensors

Transistor to Transistor
- Ultimate goal

Wafer Fab
TSV Pitch ≠ Area ÷ Number of TSVs

- TSV pitch issue example
  - 1024 bit busses require a lot of space with larger TSVs
  - They connect to the heart and most dense area of processing elements
  - The 45nm bus pitch is ~100nm; TSV pitch is >100x greater
  - The big TSV pitch means TOF errors and at least 3 repeater stages
### 3D Interconnect Characteristics

<table>
<thead>
<tr>
<th></th>
<th>SuperContact™ I 200mm Via First, FEOL</th>
<th>SuperContact™ III 200mm Via First, FEOL</th>
<th>SuperContact™ IV 200mm Via First, FEOL</th>
<th>Interposer TSV</th>
<th>Bond Points</th>
<th>Die to Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size L X W X D</strong></td>
<td>1.2 µ X 1.2 µ X 6.0µ W in Bulk</td>
<td>0.85 µ X 0.85 µ X 10µ W in Bulk</td>
<td>0.60 µ X 0.60 µ X 2µ W in SOI</td>
<td>10 µ X 10 µ X 100 µ Cu</td>
<td>1.7 µ X 1.7 µ Cu</td>
<td>3 µ X 3 µ Cu</td>
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<tr>
<td><strong>Material</strong></td>
<td></td>
<td></td>
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<tr>
<td><strong>Minimum Pitch</strong></td>
<td>&lt;2.5 µ</td>
<td>1.75 µ</td>
<td>1.2 µ</td>
<td>30/120 µ</td>
<td>2.4 µ</td>
<td>5 µ</td>
</tr>
<tr>
<td><strong>Feedthrough Capacitance</strong></td>
<td>2-3fF</td>
<td>3fF</td>
<td>0.2fF</td>
<td>250fF</td>
<td>&lt;&lt;</td>
<td>&lt;25fF</td>
</tr>
<tr>
<td><strong>Series Resistance</strong></td>
<td>&lt;1.5 Ω</td>
<td>&lt;3 Ω</td>
<td>&lt;1.75 Ω</td>
<td>&lt;0.5 Ω</td>
<td>&lt;</td>
<td>&lt;</td>
</tr>
</tbody>
</table>

*Small fine grain TSVs are fundamental to 3D enablement*
A Closer Look at Wafer-Level Stacking

Dielectric(SiO2/SiN)
Gate Poly
STI (Shallow Trench Isolation)
W (Tungsten contact & via)
Al (M1 – M5)
Cu (M6, Top Metal)

“Super-Contact”
Next, Stack a Second Wafer & Thin:
Stacking Process Sequential Pictures

Two wafer Align & Bond → Course Grinded → Fine Grinded

→ After CMP → Si Recessed

High Precision Alignment
Misalign=0.3um

Top wafer
Bottom wafer
Then, Stack a Third Wafer:
Finally, Flip, Thin & Pad Out:

1st wafer: controller

This is the completed stack!

2nd wafer

3rd wafer
3rd Si thinned to 5.5um
2nd Si thinned to 5.5um
SiO₂
1st Si bottom supporting wafer
Honeywell 0.6um SOI TSV

120K TSVs
RF, Imaging, Processing, Analog
“Dis-Integrated” 3D Memory

Memory Layers from DRAM fab

Controller Layer from high speed logic fab

2 million vertical connections per lay per die
Gen4 “Dis-Integrated” 3D Memory

DRAM layers
4xnm node

2 million vertical connections per lay per die

I/O layer contains:
I/O, interface logic
and R&R control
CPU. 65nm node

Controller layer contains: senseamps,
CAMs, row/column
decodes and test engines. 40nm node

Better yielding than 2D equivalent!
Octopus I

- 1-4Gb
- 16 Ports x 128bits (each way)
- @1GHz
  - CWL=0 CRL=2 SDR format
  - 5ns closed page access to first data (aligned)
  - 12ns full cycle memory time
  - >2Tb/s data transfer rate
- Internally ECC protected, Dynamic self-repair, Post attach repair
- 115C die full function operating temperature

Octopus II

- 4-64Gb
- 64-256 Ports x 64bits (each way)
- @1GHz
  - 5-7ns closed page access to first data
  - 12ns full cycle memory time
  - >16Tb/s data transfer rate
  - 4096 banks
  - 2+2pJ/bit
Mixing Fab, Packaging and Assembly

Foundry → ? → Packaging → ? → Assembly

? Test what where when?
Big hidden cost

Customer
Testing

- Significant planning required
- Careful analysis of yield cost
- New methodologies
  - High I/O count requires self-test
  - Deep embedding requires more effort for visibility
- Embedding memory has numerous test issues
  - Standard test interface required.
- Self-repair / Self-redundancy
2.5D Alternatives

- Silicon Interposers
  - 2-3um L/S/D
  - Rs and Cs
  - Active is the future
  - Handling & handoff

- Organics
  - 5-6 um
    - Litho limits
    - Material planarity limits
  - Great cost structure
  - TCE Challenges
  - Large substrate

- Glass
  - Large substrate
3D Choices

- **Wafer-to-wafer**
  - Best cost structure
  - Highest density interconnect
  - It’s a fab process
    - A messy fab process
      - Particles
      - Materials
      - Non-standard sizes
- **Die-to-wafer**
  - Mixed fab and packaging flow
  - Add TSVs
- **Chip-to-chip**
  - Limited interconnect
  - Cost

Increasing Cost

Increasing Complexity
>100GB, ~100B devices
New Data Needs

- Notch
- Orientation limitations
- Run out / street size / magnification
- Die location
- TCE matching / stress / warpage
  - TCE zero match at what temperature?
- Materials
- Planarity
- Surface roughness
Tezzaron/Novati 3D Technologies

- “Volume” 2.5D and 3D Manufacturing in 2013
- Interposers
- Future interposers with
  - High K Caps
  - Photonics
  - Passives
  - Power transistors
- Wholly owned Tezzaron subsidiary
- Cu-Cu, DBI®, Oxide, IM 3D assembly
Facility Overview

Capabilities

- Over 150 production grade tools
- 68000 sq ft Class 10 clean room
- 24/7 operations & maintenance
- Manufacturing Execution Systems (MES)
- IP secure environments, robust quality systems
- ITAR registered
- Full-flow 200mm silicon processing, 300mm back-end (Copper/Low-k)
- Process library with > 25000 recipes
- Novel materials (ALD, PZT, III-V, CNT, etc)
- Copper & Aluminum BEOL
- Contact through 193nm lithography
- Silicon, SOI and Transparent MEMS substrates
- Electrical Characterization and Bench Test Lab
- Onsite analytical tools and labs: SIMS, SEM, TEM, Auger, VPD, ICP-MS, etc

TRUST 2013
2.5/3D in Combination

IME A-Star / Tezzaron Collaboration

Die to Wafer Cu Thermal Diffusion Bond

μBumps

C4 Bumps

Solder Bumps

Active Silicon Circuit Board

Organic Substrate

level#0

level#1

level#2

level#3

level#4

FPGA (4Xnm)

2 Layer Processor

3 Layer 3D Memory

IME A-Star / Tezzaron Collaboration
X-ray inspection indicated no significant solder voids.

C2C sample

X-section of good micro bump

CSCAN showed no underfill voids (UF: Namics 8443-14)
Near End-of-Line TSV Insertion

TSV is 1.2µ Wide and ~10µ deep

2x,4x,8x Wiring level
~.2/.2um S/W

M8
M7
M6
M5
M4
M3
M2
M1
poly
W
STI

5.6µ
Advanced Photonic Interposers

- 2pJ/bit power target
- WDM
- Multicore fiber
- 25Gb channel interface
- Self-calibrating self-tuning
3D Key to Enable Next Gen

16nm Sea-of-Gates

14nm Sea-of-SRAM

65nm Analog and I/O

IP isolation         Optimized Process        Simplified Technology Real Reuse
Summary

- “One stop” 2.5/3D solution provider
- Open technology platform
- Volume 2.5D Si interposer production
- Volume 3D assembly
- High performance, ULP, extreme density memories
- TSV Insertion
- Silicon, 3/5 materials, carbon nanotubes
- “Fully Engineered”