Amkor Technology
Advanced Package Solutions

Robert Lanzone – SVP Engineering Solutions
Confab 2013 Las Vegas
R&D Topics

- R&D Focus

- Core Technologies

- Focus on Package Integration
R&D Focus: Profitable Growth From New Package Technologies

In the Right Markets

<table>
<thead>
<tr>
<th>Sector</th>
<th>Key Statistics</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Smartphone</strong></td>
<td>- Cumulative 5.3 Billion Unit Sales from 2012-2016 (18% CAGR)¹</td>
</tr>
<tr>
<td></td>
<td>- 59% of Handsets by 2016¹</td>
</tr>
<tr>
<td><strong>Tablet</strong></td>
<td>- Cumulative 1.1 Billion Unit Sales from 2012-2016 (27% CAGR)¹</td>
</tr>
<tr>
<td></td>
<td>- 2016 Tablet Traffic at 1.1 Exabytes per Month (Equal to Entire Global Mobile Network in 2012)²</td>
</tr>
<tr>
<td><strong>Consumer Electronics</strong></td>
<td>- Gaming Consoles</td>
</tr>
<tr>
<td></td>
<td>- “Always Connected” Devices</td>
</tr>
<tr>
<td></td>
<td>- Digital Home</td>
</tr>
<tr>
<td><strong>Networking</strong></td>
<td>- 2016 Global IP Traffic at 110 Exabytes per Month (29% CAGR from 2011)³</td>
</tr>
<tr>
<td></td>
<td>- 2016 Global Mobile Data Traffic at 11 Exabytes per Month (18-Fold Growth from 2011)³</td>
</tr>
</tbody>
</table>

¹ Gartner, Mobile Devices Forecast Update, September 2012
² Cisco Visual Networking Index Forecast, May 2012 and February 2013
³ Cisco Visual Networking Index Forecast, July 2013 and February 2013
### End Market Summary

<table>
<thead>
<tr>
<th>End Market</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Communications</td>
<td>52%</td>
</tr>
<tr>
<td>Consumer</td>
<td>19%</td>
</tr>
<tr>
<td>Computing</td>
<td>10%</td>
</tr>
<tr>
<td>Networking</td>
<td>11%</td>
</tr>
<tr>
<td>Other</td>
<td>8%</td>
</tr>
</tbody>
</table>

**Communications**
- Smartphone
- Tablet
- Wireless LAN

**Consumer**
- Gaming
- Television
- Set Top Box

**Computing**
- PC / Laptop
- Hard Disk Drive
- Peripherals

**Networking**
- Server
- Router
- Switch

**Other**
- Automotive
- Industrial

Note: Percentages represent share of LTM 1Q13 Net Sales
Mobile Communications Driving Semi Growth

**Semiconductor Industry Growth**

- **2017F - $380B**
- **Growth - $88B**
- **CAGR - 5%**

<table>
<thead>
<tr>
<th>Sector</th>
<th>2012</th>
<th>2017F</th>
<th>Growth</th>
<th>CAGR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobile Phones &amp; Tablets</td>
<td>$112</td>
<td></td>
<td>$43B</td>
<td>10%</td>
</tr>
<tr>
<td>Consumer</td>
<td>$42</td>
<td></td>
<td>$6B</td>
<td>2%</td>
</tr>
<tr>
<td>Computing</td>
<td>$74</td>
<td></td>
<td>$15B</td>
<td>6%</td>
</tr>
<tr>
<td>Networking</td>
<td>$62</td>
<td></td>
<td>$11B</td>
<td>4%</td>
</tr>
<tr>
<td>Automotive</td>
<td>$32</td>
<td></td>
<td>$7B</td>
<td>5%</td>
</tr>
<tr>
<td>Other*</td>
<td>$58</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source: Prismark Partners, February 2013

* Other includes Medical, Industrial, Military and Aerospace
R&D Focus: Customer & Market Segment

Our Product Development Focus is Based on a Clear Understanding of Each Market Segment

- Communications
- Consumer
- Computing
- Networking
- Auto / Industrial

Smartphone / Tablet:
- Applications Processor
- Digital Baseband
- Memory
- Audio Processor
- Integrated Connectivity
- Power Management
- MEMS Sensors

Infrastructure:
- Baseband ASIC
- Baseband DSPs
- Transceiver / Converter
- Power Amplifier

Brands:
- Qualcomm
- Toshiba
- Texas Instruments
- Intel
- Micron
- Samsung
R&D Focus: Critical Customer Alignment

- Samsung (25%)
- Japan Display* (20%)
- LG Display (15%)
- Sharp (10%)
- Chi Mei (10%)
- AUO (10%)

- Samsung (36%)
- Hynix (21%)
- Elpida (16%)
- Micron (13%)

- Skyworks* (34%)
- RF Micro Devices* (32%)
- TriQuint* (16%)
- Avago (7%)

- Skyworks* 30–34%
- RF Micro* 22–25%
- TriQuint* 18–19%
- Avago 5–8%
- Anadigi* 5–6%

- Atmel 26%
- Broadcom 26%
- Cypress 15%
- Synaptics* 15%
- TI 12%

- Qualcomm 40%
- TI 30%
- ST Ericsson 12%
- Maxim 6%
- Dialog Semi* 6%

- Samsung (21%)
- Toshiba (27%)
- SanDisk (19%)
- Micron (9%)

- Qualcomm (36%)
- TI (20%)
- Samsung (12%)
- Nvidia (9%)

- Qualcomm (49%)
- Mediatek (13%)
- Intel (10%)
- ST Ericsson (11%)
- Broadcom (10%)
- Marvell (9%)

- Broadcom (79%)
- TI (17%)
- Marvell (9%)

- Omnivision (30%)
- Samsung (27%)
- Apple* (55%)
- Sony (12%)
- Toshiba (9%)

- CSR* (40%)
- Broadcom (26%)
- u-blox* (26%)
- TI (9%)

Source: Gartner, Company data, Nomura estimates, * not covered by Nomura
R&D Topics

• R&D Focus

• Core Technologies

• Focus on Package Integration
Amkor’s Core Technology & Advanced Integration Schemes

- Cu Pillar
- TSV
- Thermal & Adv. Materials
- High-End FC
- WLFO
Amkor’s Core Technology & Adv. Integration Schemes

- Cu Pillar
- Thermal & Adv. Materials
- High-End FC
- TSV
- WLFO
Interconnection : Fine Pitch Cu Pillar

- **Copper Pillar Platform**
  - Foundation for most of future advanced packaging platforms
  - Potential cost reduction on substrate
  - Better electrical performance
  - Larger die in a given body size

- **Next Node Activity**
  - Reducing pitch / increasing density
  - 28/20nm in Qualification
  - Extending to all flip chip products
Executive Summary

<table>
<thead>
<tr>
<th>Driven by Demand for Handheld, High Performance, Low Power Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Provides Significant Improvement Over Solder Bump</td>
</tr>
<tr>
<td>Launched in 2010, &gt;200 Million Units Sold</td>
</tr>
<tr>
<td>Industry-Leading Platform Being Adopted by Multiple Customers</td>
</tr>
<tr>
<td>Enabling Technology for 2.5D and 3D Packaging with Through Silicon Vias</td>
</tr>
</tbody>
</table>
Why the Need for Fine Pitch Copper Pillar?

Technology Trends & Challenges

- Function Integration in All Three Dimensions
- Silicon Node “Shrinks” But Die Size Remains Unchanged or Grows
- Increased I/O Density
- Finer BGA Pitch
- More Demanding Warpage and Coplanarity Criteria

Devices

- Digital Baseband
- Applications Processor
- Networking ASICs
- Digital TV ASICs
- Power Management
Developed and Commercialized by Amkor and TI

- Early Wafer Level Copper Pillar Bumping Development
- TI Fine Pitch Development
  - Thermo Compression Assembly Development
  - Shape, Height, Pitch, Alloy, Reliability, Electromigration,…
- > 200 Million Units Sold to Date
  - Multiple Customers in Production or Qualification

- 2004
  - New Copper Chemistry Developed
- 2006
- 2008
- 2010
- 2012
  - Product Launch in Conjunction with Texas Instruments
Creation of Cu Pillar

- Sputtered Seed Layer (TiWCu)
- Resist Coat
- Expose and Develop
- Plate Cu/Solder (SnAg)
- Strip Resist
- Seed Layer Etch
- Reflow Solder
Thermo-Compression Bonding (TCNCP) Animation

1. NCP writing
2. Bond force then head temperature is going up to solder melting point: 220
3. Bond Head up: Bonding completed

NCP, Cu pillar, Die, PCB, Bump pad, Solder, NCP
Amkor’s Core Technology & Adv. Integration Schemes

- Cu Pillar
- TSV
- Thermal & Adv. Materials
- High-End FC
- WLFO
Integration: Through Silicon Via (TSV)

• **Current Status**
  ✓ World’s first mass production of TSV backside finishing
  ✓ World’s first production of fully integrated TSV package platform
  ✓ “Logic dies on Si interposer” product is being produced
  ✓ ~10 customers are engaged in active TSV development
  ✓ Target devices
    ▪ Logics on Si interposer
    ▪ Logics + memories on Si interposer
    ▪ Memory / Memory stack
    ▪ Memory / Logic combination
Focus: Provide Most Cost Effective / Reliable Option

**Chip on Substrate**
- **“Co-CoS”**
  - Positives
    - Leverages Std FC Process
    - Allows Interim Test
    - Many Assy Options
  - Negatives
    - Most Difficult Die Join Last
    - Warpage of Interposer
    - Warpage of Substrate

**Chip on Wafer**
- **“CoW-oS”**
  - Positives
    - Most Difficult Connect First
    - May Eliminate WSS
    - Flat Surface for Assy
  - Negatives
    - Commits Expensive BOM
    - Saw Street Growth
    - No Opp’ty for Interim Test

**Chip on Chip**
- **“CoC-oS”**
  - Positives
    - Most Difficult Connect First
    - KGD assembly
    - Many Assy Options
  - Negatives
    - Commits Expensive BOM
    - Warpage of Interposer
    - No Opp’ty for Interim Test

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2.5D TSV & Interposer Supply Chain

- **High End Products**: Networking, Servers
  - Silicon interposers; < 2um L/S, < 15nsec latency, > 25k µbumps per die
  - Amkor is engaged with Foundries to deliver silicon interposers today

- **Mid Range Products**: Gaming, Graphics, HDTV, Adv. Tablets
  - Silicon or Glass interposers; < 3um L/S, < 25nsec latency, ~10k µbumps/die
  - Glass may provide cost reduction path in future
  - Not actively pursuing glass interposers yet as infrastructure still immature

- **Lower Cost Products**: Lower End Tablets, Smart Phones
  - Silicon, Glass or Laminate interposer; < 8um L/S, low resistance, ~2k µbumps
  - Must provide cost reduction path to enable this sector
  - Working with laminate supply chain to enable
TSV Production Intercepts

- **ASIC, GPU, CPU** (28 - 20nm)
  - Interposer required all Platforms
    - Logic^T + SDR or DDR3^T

- **Apps Processor** (28 - 20nm)
  - Interposer required for some platforms
    - Logic^T + SDR or DDR3^T

- **Custom Mem** (45 & 32nm)
  - Stacked DDR^T ... or on Logic

- **ASIC, FPGA** (28nm)
  - Logic on Si Interposer^T

- **WLCSP** (28nm)
  - Production Since Nov ‘11

- **Production Since ‘10**

- **RFPAT**

Die with TSV indicated by = T

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Reliability & Trust
Amkor’s Core Technology & Adv. Integration Schemes

- Cu Pillar
- TSV
- Thermal & Adv. Materials
- High-End FC
- WLFO
Advanced Platform: Wafer Level Fan Out (WLFO)

- WLFO is now established as a viable alternative to conventional laminate-based and wafer-based packages.
- The elimination of a conventional laminate substrate and utilization of wafer-level packaging’s advanced design and feature size capabilities provide many benefits for WLFO, including:
  - Increased I/O density
  - Reduced form factor (including z-height)
  - Improved electrical and mechanical performance
  - Multi-chip capability
  - Outstanding performance capability
  - Scalability within a heterogeneous assembly platform
  - Opportunity for advanced 3D structures
• WLFO reached the $100M market valuation in 2011
• Predicted by Yole to reach $250M market valuation in the 2015/16 timeframe once demand moves from IDMs to fabless wireless IC players and the OSAT supply chain expands
Amkor Embedded Die Strategy

- All future technology roadmaps indicate a need for higher levels of integration, thinness and cost effective solutions
  - Embedded die will be a key enabling package technology that addresses these roadmap requirements
- Amkor already supports embedded die in substrate
  - Passive integration in high volumes already
  - Active integration just starting
- Amkor has made strategic decision to focus newest efforts in this space on a ‘Panel Level Fan-Out’ platform to address cost, integration and scalability
- Embedded die resources now focused on Panel platform development
Evolution of WLFO

- **Key enabling technologies for extensions into 3D**
  - Thru Mold Via (TMV®)
  - Fine pitch copper pillar
  - CoC possum™
Amkor’s Core Technology & Adv. Integration Schemes

- Cu Pillar
- TSV
- Thermal & Adv. Materials
- High-End FC
- WLFO
Flip Chip & Advanced Packaging Leader

- Migration to Flip Chip, 3D and Advanced Packaging Continues to Accelerate
- Driven by Strong Demand for Smartphones, Tablets, Consumer Electronics, Network Infrastructure
- Enhances Device Performance, Reduces Power Consumption and Form Factors
- Higher Gross Margin and Returns Versus Wirebond

LTM 1Q13 Flip Chip & Advanced Packaging Revenue

Non-Amkor Sources: Company Press Releases
Adv. Packages : High Performance Flip Chip

• **Production Status**

✓ Increasing body size (>55mm BD)
✓ Increasing die size (>26mm)
✓ 45/40nm in HVM, 32/28nm in AVM
✓ Full lead free qualified at 65, 45/40, and 32/28nm
✓ Cu Pillar for below 150um bump pitch
✓ Molded FCBGA in AVM
✓ Coreless substrate under development for 32/28nm
Adv. Packages : Molded U/F FCBGA (FCmBGA)

- **Production Status**
  - ✓ Increasing body size (~45mm BD)
  - ✓ Increasing die size (~26mm)
  - ✓ 40/28nm in LVM
  - ✓ Eutectic & Lead-free qualified at 40/28nm
  - ✓ Eutectic & Lead-free & Cu pillar for min 150um bump pitch
  - ✓ Thin core under development (<0.4mm) substrate for 32/28nm
Advanced FC Packages: Chip on Chip

- Next Generation of FC – CoC_{POSSUM}
  - MEMs, Automotive, Networking
Advanced FC Packages: Chip on Chip, cont.

- 2014 targeted production
Amkor’s Core Technology & Adv. Integration Schemes

- Cu Pillar
- TSV
- High-End FC MUF
- WLFO

Thermal & Adv Materials

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Advanced Packaging & Technology Integration

Adaptive Learning Required

Copper μPillar Bumping

Die Joining

Underfill

Thermal

Sub-assembly & Package Warpage
Amkor’s Advanced Materials

Enabling the Future
Amkor’s Advanced Materials

- Thermal Performance

- Epoxy Mold Compound
  - 3W/mK
  - 5W/mK
  - 8W/mK

- Die Attach Paste
  - L/F (Ag paste)
  - L/F (Sintered paste)
  - BGA
  - 4W/mK
  - 10W/mK
  - 20W/mK
  - 1W/mK
  - 2W/mK
  - 5W/mK
  - 10W/mK
  - 60W/mK
  - 20W/mK

- Die Attach Film (BGA)
  - 1W/mK
  - 2W/mK
  - 5W/mK

- TIM (Flip Chip)
  - 4W/mK
  - 6W/mK
  - 10W/mK

- Underfill Material (FC)
  - 0.5W/mK
  - 1W/mK
  - 1–2W/mK

* Thermal conductivity is bulk value of the material, not actual package thermal performance.
Amkor’s Advanced Materials

- Molded Underfill (MUF)
  Target package type : FCmBGA

### Die
- Bump Alloy
- Si Node
- Bump Pitch (C)
- Bump Gap (D)

<table>
<thead>
<tr>
<th></th>
<th>Current</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bump Alloy</td>
<td>EU</td>
<td>Pb free / Cu pillar</td>
<td>28/32nm</td>
<td>22nm</td>
</tr>
<tr>
<td>Si Node</td>
<td>28/32nm</td>
<td>28/32nm</td>
<td>130um</td>
<td>&lt;120um</td>
</tr>
<tr>
<td>Bump Pitch (C)</td>
<td>150um</td>
<td>130um</td>
<td>40um</td>
<td>&lt;35um</td>
</tr>
<tr>
<td>Bump Gap (D)</td>
<td>60um</td>
<td>50um</td>
<td>50mm</td>
<td>400um</td>
</tr>
</tbody>
</table>

### Package
- Die Size (A)
- Mold edge to substrate (B)
- PKG size (D)

<table>
<thead>
<tr>
<th></th>
<th>Current</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size (A)</td>
<td>19x16mm</td>
<td>20x22mm</td>
<td>&gt;22mm</td>
<td></td>
</tr>
<tr>
<td>Mold edge to substrate (B)</td>
<td>600um</td>
<td>500um</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PKG size (D)</td>
<td>45mm</td>
<td>50mm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Amkor’s Advanced Materials

- **Next Generation Underfill Development Strategy**
  - **Capillary Based (continuous):**
    - ✓ High modulus and superior adhesion; good flowability & low warpage
  - **Film Based:**
    - ✓ Pre-coated non-conductive film underfill material on wafer
R&D Topics

- R&D Focus
- Core Technologies
- Focus on Package Integration
Amkor Advanced Package Integration

Interconnect Density & Functionality: Increasing
Package Migration to 3D & SiP-MCM Integration

2.5D MCM - CPU, GPU, Networking
- 100X Improvement in Inter-Die Bandwidth / Watt
- 50% Power Savings
- 5X Latency Reduction
- 20X denser Wire Pitch

3D - Smartphones, Tablets, Memory
- 8X Performance in Bandwidth
- 50% Power Savings
- Profile Improvement
Amkor Advanced Package Integration Roadmap

Production

Transition

Developing

Interconnect Density & Functionality: Increasing
Industry Advanced Package Integration Roadmap

Current / Future Tool-Box for 3D Packaging

- TSV
- WLP
- Embedded die
- BGA/PoP
- 3-D Logic SiP
- 3-D Flip-Chip
- 3D Silicon PoP
- 3D RF-SiP
- FO PoP
- FO MCP
- Embedded MCP Module
- MEMS & sensors WLP
- WLP Fan-in

Commissioned report September 2011 courtesy of Amkor Technology and Yole Développement

Chip / Package Size

2mm²
30mm²
50mm²
80mm²
100mm²
500mm²

2011 • 93

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Thank You!