ChipsetT™ Embedded Die Packaging: The Next Step in Enabling 3D System in Package Miniaturization

Theodore Tessier, Jon Aday, David Hays, Kazuhisa Itoi* and Satoshi Okude*

FlipChip International, LLC
Phoenix, AZ, USA

Fujikura Electronic Device Laboratory*
Sakura, Chiba, Japan
Embedded Die Packaging: What is it?

- Embedded Die Substrate Technology
  - Embedding active and passive components into the substrate

- What problems does it solve?
  - Form factor reduction
  - Product integration
  - Better signal control by getting components closer together

- Requirements:
  - Cu terminated actives and passives
  - Known good die
  - Target 100% substrate yield to minimize loss of KGD
  - Proper design to get the heat out
Embedded Die Packaging Configurations

Fan Out CSP

Embedded Die SiP

Package on Package (PoP 3D Solution)

WLCSP
This packaging technology leverages Wafer Level processing know how and Multilayer embedded die flex circuit technology

Next Generation Chip Embedding Solutions
Fan-In Wafer Level Redistribution for Ease of Die Embedding

+> Eases large panel die placement requirements.

+> Relaxes laser via tolerance requirements.

+> Highest efficiency of highest density routing (RDL)

+> Higher overall yields!!

+> Lowest cost option for finest interconnects (highest density)
High Level Embedded Fabrication Flow

- Embedded IC
  - Wafer Level Packaging process
    - Forming RDL
    - Backgrinding (thinning) Singulation

- Wiring board
  - Flexible printed circuit process
    - Forming copper circuits
    - Opening via hole
    - Proprietary Via Fill Technology

- Co-laminating
  - Layer Stack
  - Lamination

- Backend processing
  - Bumping, Marking, Singulation
Embedded Die Fabrication Process (Co-lamination)

- Stack and Alignment
- Embedding IC
- Press and Heat
- Adhesive
- Conductive paste
- Solder Mask
Low Profile Flex Based Embedded Die Package Stack-Up Details

Thinned WLP : 85\(\mu\text{m}\)
Adhesive film : 25\(\mu\text{m}\)
PI film : 25\(\mu\text{m}, 50\mu\text{m}\)
Cu foil : 12\(\mu\text{m}, 18\mu\text{m}\)

Body Thickness = 240\(\mu\text{m}\) (4 metal layers)
Optical Image (front side)  Optical Image (back side)

SEM Cross-sections of Chiplet™ Fan-Out CSP
Process Simplicity + Panel Efficiency

- > 3500 modules/panel (4.5 x 4.5mm)
- Single Panel Lamination Step
- Panel Size Extendibility
  - 250 x 350mm (current)
  - 350 x 500mm (2013)
# Multilayer Flex Embedded Die Package Design Guidelines

## Non-molded

- Adhesive IC
- Polyimide
- Via
- Solder mask

## Overmolded

- Mold Cap

<table>
<thead>
<tr>
<th>Item</th>
<th>Design Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Lamination Layers</td>
<td>7 PI layers</td>
</tr>
<tr>
<td>Package body profile (exc. Bump)</td>
<td>240 µm @4 PI layers</td>
</tr>
<tr>
<td>Min Line/Space of Cu circuit</td>
<td>30 / 30 µm (Sub.)</td>
</tr>
<tr>
<td></td>
<td>20 / 20 µm (Semi.)</td>
</tr>
<tr>
<td>Min Pad Pitch - embedded IC</td>
<td>60µm</td>
</tr>
<tr>
<td>Max embedded component thickness (die and passives)</td>
<td>150µm</td>
</tr>
<tr>
<td>Overmold with SMT components</td>
<td>Yes</td>
</tr>
</tbody>
</table>

06/24/2013
Embedded Passive Options

Passive component

With Cu terminations

Conductive paste via

<table>
<thead>
<tr>
<th>Sizes (mm)</th>
<th>Thickness (um Max)</th>
<th>Capacitance Values (uF)</th>
<th>Voltage (V)</th>
<th>Temp. Efficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>0603</td>
<td>150</td>
<td>0.1 – 0.22</td>
<td>2.5 – 10.0</td>
<td>X5R, X6S, X7S, X7T</td>
</tr>
<tr>
<td>1005</td>
<td>150</td>
<td>0.022 – 1.0</td>
<td>2.5 – 6.3</td>
<td>X5R, X6S, X7S, X7T</td>
</tr>
</tbody>
</table>
Embedded Passive Constructions

Cross-sectional structure

Conductive paste via

<table>
<thead>
<tr>
<th>Total Thickness</th>
<th>260 µm (5 wiring layer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Embedded passive components dimensions</td>
<td>1.0 mm x 0.5 mm x 150 µm (M1005 size)</td>
</tr>
<tr>
<td></td>
<td>0.6 mm x 0.3 mm x 150 µm (M0603 size)</td>
</tr>
<tr>
<td>Type of passive components</td>
<td>Jumper Resistors (0 Ω)</td>
</tr>
<tr>
<td>Embedded WLP-IC dimensions</td>
<td>3 mm x 3 mm x 85µm</td>
</tr>
<tr>
<td>Interstitial via diameter</td>
<td>100µm</td>
</tr>
</tbody>
</table>
## Package Reliability: CSP50 Test Vehicle Details

<table>
<thead>
<tr>
<th>Test Component</th>
<th>ChipletT CSP 50</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pitch</strong></td>
<td>0.5 mm, 0.3mm Ball diameter</td>
</tr>
<tr>
<td><strong>Array Size</strong></td>
<td>Full Array 10 x 10 98 I/O</td>
</tr>
<tr>
<td><strong>I/O Pad</strong></td>
<td>Cu</td>
</tr>
<tr>
<td><strong>Component Size</strong></td>
<td>5 mm x 5mm x 0.45 mm</td>
</tr>
<tr>
<td><strong>Package Body Thickness</strong></td>
<td>260 um</td>
</tr>
<tr>
<td><strong>Bump height</strong></td>
<td>190 um</td>
</tr>
<tr>
<td><strong>Silicon Die Thickness</strong></td>
<td>70 um</td>
</tr>
</tbody>
</table>
# Embedded Package Reliability Data

<table>
<thead>
<tr>
<th>Type of Test</th>
<th>Test Conditions</th>
<th>Test Conditions</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL Level 1</td>
<td>85°C at 85% rHFollowed by 3x reflows at 250°C peak</td>
<td>168 Hours</td>
<td>Pass</td>
</tr>
<tr>
<td>High Temperature Storage (HTS)</td>
<td>150°C</td>
<td>1000 Hours</td>
<td>Pass</td>
</tr>
<tr>
<td>Low Temperature Storage (HTS)</td>
<td>-40°C</td>
<td>1000 Hours</td>
<td>Pass</td>
</tr>
<tr>
<td>Multiple Reflow</td>
<td>Standard Reflow profilePeak Temperature 250°C</td>
<td>10x Reflows</td>
<td>Pass</td>
</tr>
<tr>
<td>Component Level Temperature Cycling</td>
<td>-40°C to 125°C</td>
<td>1000 Cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>Humidity Temperature no bias</td>
<td>85°C, 85%</td>
<td>1000 Hours</td>
<td>Pass</td>
</tr>
<tr>
<td>U-HAST</td>
<td>130degC, 85%(2 atm)</td>
<td>336 Hours</td>
<td>Pass</td>
</tr>
<tr>
<td>Autoclave</td>
<td>121°C at 100% Relative Humidity</td>
<td>168 Hours</td>
<td>Pass</td>
</tr>
</tbody>
</table>

**Acceptance Criteria:**

**Appearance:** no signs of voiding, no delamination.

**Circuit resistance change:** less than 20% change from $t=0$
JEDEC Drop Test Results: CSP50 Package

Drop Test
- Sample Size - 5 boards (1 board for first failure analysis)

Drop Test Results
- First Failure - 116 drops
- Characteristic Life - 300 drops

CSP50 Test Board

β=3.0332, η=300.3249, ρ=0.9562


30 drops
Embedded Die Thermal Solutions

Face-down
No Thermal via

Face-down
With Thermal via

Face-up
With Thermal via

Proprietary Via Technology
Simulated & Experimental Thermal Performance

Face-down Embedded Die, Without Thermal Vias (reference)

<table>
<thead>
<tr>
<th></th>
<th>Without thermal via</th>
<th>With thermal via</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Experimental</td>
<td>Simulation</td>
</tr>
<tr>
<td>$\theta_{jc}$</td>
<td>14 °C/W</td>
<td>15 °C/W</td>
</tr>
</tbody>
</table>
Challenges Remain

- Key Objective for Longer Term Roadmap
- Cost Reductions
Typical Fan-Out CSP Application

Application Details:

- **Body Size:** 2.2 mm x 2.6 mm
- **Bump Pitch:** 0.4 mm
- **I/O Count:** 29 I/O
- **Overall Package Thickness:** 460 um (260 um thick package substrate; 200 um bump)
- **Number of packages per panel:** 2538
- **140 mm x 140 mm panel size enables panel level testing of packaged devices using customer’s existing 200 mm diameter WLCSP test infrastructure**
GaAs Packaging: Ruggedizing Fragile Devices

Application Details:
- 1 embedded EDC die without mold cap
- 8 I/O, 0.4mm pitch bumps
- Depopulated 3 x 3 array
- Enables standard SMT handling of fragile GaAs Devices

Embedded Die Layer Sketch

ChipletT Bump Layout

Stack Up Drawing (not to scale)
CSP Package Layout
Footprint Matching

- 1 Embedded die
- 6 I/O pads, 0.65mm pitch, BGA

Package Footprint Modification

Application Details:
- 4 I/O Device modified using ChipletT Packaging to enable a 6 I/O package footprint compatible with competitor’s WLCSP package option.
- 300 micron diameter solder spheres
- 4 week Cycle Time to prototypes!!

<table>
<thead>
<tr>
<th>Package Size</th>
<th>2.3 mm x 1.7 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Thickness</td>
<td>340 µm</td>
</tr>
<tr>
<td>Die Size</td>
<td>1.1 mm x 1.3 mm</td>
</tr>
<tr>
<td>Pad Pitch</td>
<td>0.65 mm</td>
</tr>
<tr>
<td>Pad Opening</td>
<td>310 µm</td>
</tr>
<tr>
<td>Pad Finish</td>
<td>Cu-OSP</td>
</tr>
</tbody>
</table>

06/24/2013
- Expose the die to allow direct silicon exposure to light or other stimuli
- Currently defining the adhesive bleed onto the die surface

Exposed Area

Adhesive flow

1 x 3 mm cavity

Exposed Area
Typical Embedded Die System in Package (SIP)

Conventional (3.5 mm x 3.5 mm)

ChipsetT(2.5 mm x 2.5 mm)
1 chip embedded, 4 chips SMT

50% footprint reduction!

Cross-sectional photograph of overmolded package
### Area and Volume Reduction Enabled by Embedding

<table>
<thead>
<tr>
<th>Package Structure/Application</th>
<th>(mm^2)</th>
<th>Original Design</th>
<th>ChipsetT Design</th>
<th>% Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEMS Module</td>
<td>X-Y Area</td>
<td>17.7</td>
<td>7.0</td>
<td>60%</td>
</tr>
<tr>
<td></td>
<td>Volume</td>
<td>21.7</td>
<td>7.9</td>
<td>64%</td>
</tr>
<tr>
<td>Power Module</td>
<td>X-Y Area</td>
<td>36.0</td>
<td>30.5</td>
<td>15%</td>
</tr>
<tr>
<td></td>
<td>Volume</td>
<td>32.4</td>
<td>9.6</td>
<td>70%</td>
</tr>
<tr>
<td>Power Module</td>
<td>X-Y Area</td>
<td>36.0</td>
<td>21.5</td>
<td>40%</td>
</tr>
<tr>
<td></td>
<td>Volume</td>
<td>32.4</td>
<td>9.9</td>
<td>69%</td>
</tr>
<tr>
<td>Control Module</td>
<td>X-Y Area</td>
<td>22.3</td>
<td>16.5</td>
<td>26%</td>
</tr>
<tr>
<td></td>
<td>Volume</td>
<td>54.7</td>
<td>20.3</td>
<td>63%</td>
</tr>
<tr>
<td>Control Module</td>
<td>X-Y Area</td>
<td>16.0</td>
<td>7.3</td>
<td>54%</td>
</tr>
<tr>
<td></td>
<td>Volume</td>
<td>16.0</td>
<td>7.5</td>
<td>53%</td>
</tr>
</tbody>
</table>

39% Average Area Reduction!
64% Average Volume Reduction!
Multilayer Flex Embedded Die Medical Module

Primary Technical Driver: **Form Factor Reduction!**
(26% area reduction; 63% volume reduction)

**Bill of Materials:** 1 DSP, 1 EEPROM, 14 passives

- Concurrent RDL & Substrate Design!
- 3D Module Design
Partially Assembled Medical Module Assembly

- **Primary Technical Driver:** Form Factor Reduction
  - (26% area reduction; 63% volume reduction)
- Double Sided SMT
- Single Embedded Die

![Bumped WLCSP Image]
Low Profile Package on Package Embedded Die Assembly

Schematic of Package on Package (PoP) Assembly

No limitation on location of top package BGA balls

Package on Package (PoP) Embedded Die Solution
Stacked Die Embedded Package
• Demand for **ultra thin**, fine pitch, **stackable (3D)** packaging solutions for handheld product applications continues....

• Flex based embedded die packages provide attractive options by combining mature, **HVM proven flex circuit manufacturing**, component embedding and wafer level RDL processing.

• Embedded die packages meet and exceed industry standard component level and board level **reliability requirements**. Work is in progress to characterize package body sizes up to 12 mm x 12 mm.

• Embedded die packaging enables **heterogeneous integration**, thus opening up new opportunities for innovative packaging solutions.