Hetero-integrations for Adaptive Compute Acceleration Platform

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Three Big Trends

1. Explosion of Data
   - 90% unstructured
   - Video & image content
   - Needs higher throughput & real-time computing

2. Dawn of AI
   - Adoption across all industries
   - Injecting new intelligence into apps
   - From endpoints to edge to cloud

3. Computing After Moore’s law
   - Heterogeneous computing with accelerators
   - Breadth of apps require different architectures
   - Speed of innovation outpacing silicon cycles
Accelerate Core Vertical Markets

- Automotive
- Wireless Infrastructure
- Wired Communications
- Audio, Video, & Broadcast
- Aerospace & Defense
- Industrial, Scientific & Medical
- Test, Measure, & Emulation
- Consumer
Flexibility of Programmable Hardware with Design Tools

Enables Full Programmability for Software Developers
- CPU and GPU-like development environments
- Automated software acceleration in programmable logic

15X Productivity for Hardware Developers
- Graphical plug-and-play IP Integration
- High Level Synthesis in C, C++, and System C

State-of-the-Art Tools for Traditional Hardware Design
- Optimizes for performance, low power, and density
- Advanced flows in-system updates and remote debug
Transformation Through Innovation

- World's 1st FPGA
- Virtex FPGA
- World's 1st 2.5D FPGA & Zynq
- SDx, RAS, ReVision MPSoC, Hood, RFSoC
- Vivado MPSoC, Hood, RFSoC
- Virtex-2 Pro

Timeline:
- 1980
- 1990
- 2000
- 2010
- 2020

Next Generation

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Driving Adaptive Computing with a New Device Category
Adaptive Compute Acceleration Platform (ACAP)

Dynamically Adaptable to Workloads
- Adapts with programmable fabric
- Dynamic reconfiguration for diverse applications

Exponential Increase in Acceleration
- 20X AI compute capability
- 4X communication bandwidth for 5G

Fully Software Programmable
- Network-on-Chip & SW/HW accelerations engines
- Ease-of-programming for both HW and SW developers

Project Everest: World’s First 7nm ACAP
Comprehensive SoC Portfolio

Heterogeneous Processing for Autonomous Embedded Systems
Embedded Vision • Automotive • Industrial • Edge Compute • Multi-Level Safety & Security

Single to Dual-Core ARM
Multi-Core, Multi-Processing ARM
Integrated RF Subsystem

Zynq-7000 SoC
Zynq UltraScale+ MPSoC
Zynq UltraScale+ RFSoC
3D-IC: Technology Hetero-integration

Connection (bump) density: $\frac{1}{(\text{bump pitch})^2}$ (1/mm$^2$)

Routing density: $\frac{1}{\text{(line pitch)}}$ (1/um)

- Glass interposer
- Fine-pitch
- CoWoS / Si interposer
- Cu/SiO2 fusion bounding
- Flipchip MCM
- EMIB